IN THE DRAWINGS:

Please amend Figure 12 by changing "A[L]" to "T[L]" in the box labeled S353. A replacement sheet for Figure 12 is included herewith.

REMARKS

I. Introduction

In response to the Office Action dated January 3, 2006, Applicants have amended claims 4, 6, and 11 to more particularly point out and distinctly claim the subject matter of the invention. Claims 1 – 3, 5 , 7 – 10, and 12 – 18 have been canceled and claims 19 – 21 have been added.

Applicants have also amended the specification to correct the minor informalities indicated in the Office Action. Additionally, Figure 12 has been amended to correct a typographical error by changing "A[L]" to "T[L]" in the box labeled S152. No new matter has been added. In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Claim Rejection Under 35 U.S.C. § 112

Claim 4 stands rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to meet the written description requirement. Claims 6 – 8 stand rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the enablement requirement. Claims 2 – 10, 13, and 16 – 18 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. Applicants traverse these rejections for at least the following reasons.

Regarding claim 4, the Examiner first asserts that there does not appear to be any disclosure of how the value that is added to the access frequency index is obtained and whether it is different depending on the type of access. However, this is fully illustrated in Figure 12 and the accompanying portions of the specification describing Figure 12 (see pages 37 – 38).

In the case where data is only cached to the cache memory from the FERAM without being written back (dirty bit is not set to "1"), the array element T[L] is modified to "1", as

depicted at S138 in Figure 12. On the other hand, in the case where data is cached to the cache memory from the FERAM and later written back to the FERAM (dirty bit is set to "1"), the array element T[L] is modified to "2", as depicted at S136. The resulting value of T[L] is added to the access frequency index, as depicted at S353. Thus, in the case where data is cached from the FERAM, the value "1" (i.e., the first value recited in claim 4) is added to the access frequency index and the value "2" (i.e., the second value recited in claim 4) is added to the access frequency index in the case where data is cached from and written back to the FERAM. Accordingly, as every feature of claim 4 is clearly described in the specification, which includes the drawings, claim 4 meets the written description requirement of § 112, first paragraph, and withdrawal of this rejection is respectfully requested.

Claim 4 has also been rejected as allegedly being indefinite. Specifically, the Examiner asserts that claim 4 includes the limitation "an access frequency index" on lines 4 and 7 while claim 1 already provides "an access frequency index" on line 12. It is the Examiner's position that it is unclear whether the recited access frequency index in claim 4 is the same as that of claim 1. Claim 4, which is now in independent form including all of the limitations of now canceled claims 1 and 2, has been amended to recite "the access frequency index" after the first recitation, indicating that this is the same access frequency index first recited in the claim. Accordingly, withdrawal of the rejection under § 112, second paragraph, is respectfully requested.

Regarding claim 6, the Examiner first asserts that claim 6 discloses a management apparatus that performs wear leveling that is unclear based on the Examiner's understanding of wear leveling and the invention as disclosed. The Examiner is referred to Figure 6 and to embodiment 1 of the invention. First, the cache access frequency index is set to "0" as depicted

at S139 in Figure 6. Each time the cache data is accessed, the value stored in the cache access frequency index column 124 is incremented by "1" (see Specification at page 22, lines 22 – 24). If the cache access frequency index is greater than the access frequency index, the cache access frequency index is updated so as to hold the value of the access frequency index, as depicted at S134. Accordingly, as every feature of claim 6 is described in such a manner as to enable one of ordinary skill in the art at the time of the invention to make and use the invention, claim 6 meets the enablement requirement of 35 U.S.C. § 112, first paragraph, and withdrawal of this rejection is respectfully requested.

The Examiner also asserts claim 6 recites the limitation "a cache frequency index" on line 8 and also recites "a cache access frequency index" on line 3 of the claim, making it unclear whether the recitations refer to the same element. Claim 6, which is now in independent form including all of the features of now canceled claims 1 and 2, has been amended to refer to "the cache access frequency index" after the first recitation, indicating that this is the same cache access frequency first recited in the claims. Accordingly, withdrawal of the rejection under 35 U.S.C. § 112, second paragraph, is respectfully requested.

Claims 2, 3, 5, 8 – 10, 13, and 16 – 18 have also been rejected under 35 U.S.C. § 112. However, as these claims have been canceled, these rejections are now moot. To the extent that the features previously presented in these claims have been included in the currently pending claims by amendment, any relevant rejection of these features have been addressed in the foregoing amendments.

III. Claim Rejections Under 35 U.S.C. § 101

Claims 6 – 8 stand rejected under 35 U.S.C. § 101 as allegedly lacking patentable utility. Applicants traverse this rejection for at least the following reasons. The memory management

apparatus of claim 6 holds a peak value of the access frequencies of each logical page such that a logical page once recorded with a high peak value is mapped to a less degraded physical page thereafter. As recited in the specification at page 10, beginning at line 5, the structure as recited in claim 6 is especially suitable in cases where a specific logical page is accessed intensively over a long term because such a frequently accessed logical page is mapped to a least degraded physical page without regard to short-term fluctuations in the access frequencies. Thus, claim 6 clearly has utility and withdrawal of this rejection is respectfully requested.

IV. Claim Rejections Under 35 U.S.C. § 102

Claims 1 and 15 stand rejected under 35 U.S.C. § 102(a) as allegedly being anticipated by applicant's allegedly admitted prior art. Claims 1 and 15 have been canceled. Accordingly, the rejection of these claims is now moot.

V. Claim Rejections Under 35 U.S.C. § 103

Claims 2 – 5, 9 – 11, 16, and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Applicant's allegedly admitted prior art in view of U.S. Patent No. 6,000,006 to Bruce in view of U.S. Patent Publication No. 2003/0058681 to Coulson. Claims 12, 13, and 18 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Applicant's allegedly admitted prior art in view of Bruce and U.S. Patent Publication No. 2004/0243671 to Bohrer. Claim 14 stands rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Applicant's allegedly admitted prior art in view of Bruce, Bohrer, and Coulson. Applicants traverse these rejections for at least the following reason.

Claims 2, 3, 5, 9, 10, 16, and 17 have been canceled. Accordingly, the rejection of these claims is now moot.

Claim 4 recites, among other things, an access frequency index updating unit operable to add the first value to an access frequency index of a logical page that is mapped according to the mapping information to each physical page retaining original data of cache data stored in the cache storage unit, and to add the second value to an access frequency index of a logical page that is mapped according to the mapping information to each physical page to which modified cache data has been written back. At least this feature is not taught or suggested by any of the cited references, alone or in combination with each other.

As described above, in the case where data is cached from the FERAM, the value "1" (i.e., the first value recited in claim 4) is added to the access frequency index and the value "2" (i.e., the second value recited in claim 4) is added to the access frequency index in the case where data is cached from and written back to the FERAM. Degradation degree differs depending upon whether data is only cached from the FERAM to the cache memory or data is cached from the FERAM to the cache memory and written back to the FERAM. By selecting a value to be added to the access frequency index based on the type of access, the FERAM undergoes memory degradation evenly over its memory area rather than intensively at a specific location. The Examiner admits that the admitted prior art does not disclose this feature, and relies on Bruce and Coulson to overcome these deficiencies. However, neither reference discloses or implies that a different value is added to the access frequency index of a logical page, depending on the type of access made to the logical page, as recited in claim 4.

The Examiner relies on Bruce as allegedly teaching a method of wear leveling wherein frequently written data is stored in a cache and written back at certain time intervals and write counters are used to track the total number of writes to a physical block. The Examiner relies on Coulson as allegedly disclosing a counter that keeps tracks of both reads and writes. However,

even if these features were taught by the cited references, none of the references disclose or suggest adding a ***different value*** to the access frequency ***depending upon the type of access*** made to the logical page.

Accordingly, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (MPEP § 2143.03), and the combination of Applicant's allegedly admitted prior art, Bruce, and Coulson fails to do so, it is respectfully submitting that claim 4 is patentable over the cited references taken alone or in combination with one another.

Claim 11 depends from one of claims 4 or 6. Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as claims 4 and 6 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

New claims 19 and 20 recite features similar to claims 4 and 6. Accordingly, claims 19 and 20 are patentable at least for the reasons provided above in reference to claims 4 and 6.

VI. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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